How to implement and connect between an Altera_PLL and ALTLVDS_RX with DPA feature megafunction in external pll mode for Arria® V and Stratix® V devices

Introduction

In the Quartus® II software version 12.1 and onwards you will encounter an error during Analysis and Synthesis when using ALTLVDS RX in external PLL mode with DPA enabled and any of the following options are turned on in the Altera_PLL megafunction:

- Enable dynamic reconfiguration of PLL (Altera_PLL)
- Enable access to dynamic phase shift ports
- Enable physical output clock parameters

The following guide will describe how to fix this error for Arria V and Stratix V devices.

1. Set Up

The examples in this document use the following:

- Quatus II software version 12.1
- Altera_PLL megafunction
- ALTLVDS_RX megafunction
- ALTLVDS_TX megafunction

2. Background

Figure 2-1 shows the typical connection when using the ALTLVDS_RX and ALTLVDS_TX megafunctions in external PLL mode.

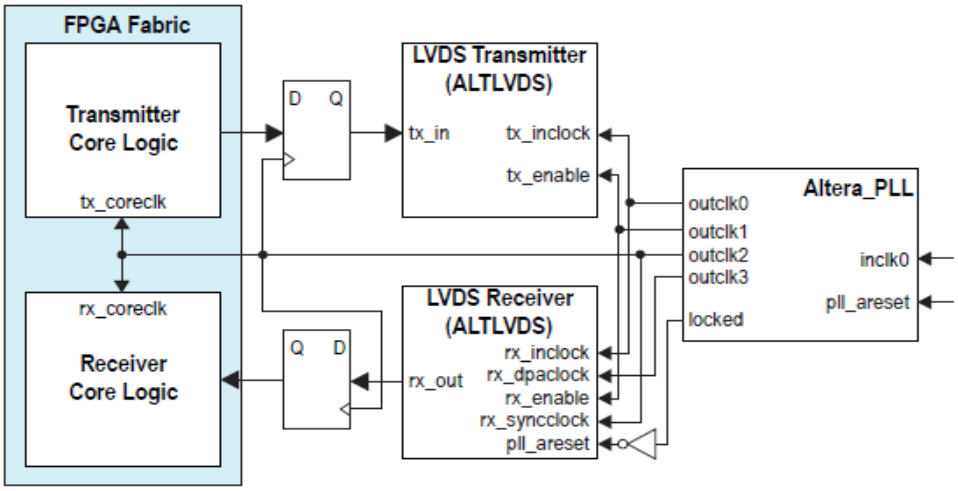

Figure 2-1. LVDS Interface with the Altera_PLL Megafunction (With DPA)

Figure 2-2 shows enabling of dynamic reconfiguration in the Altera _PLL megafunction.

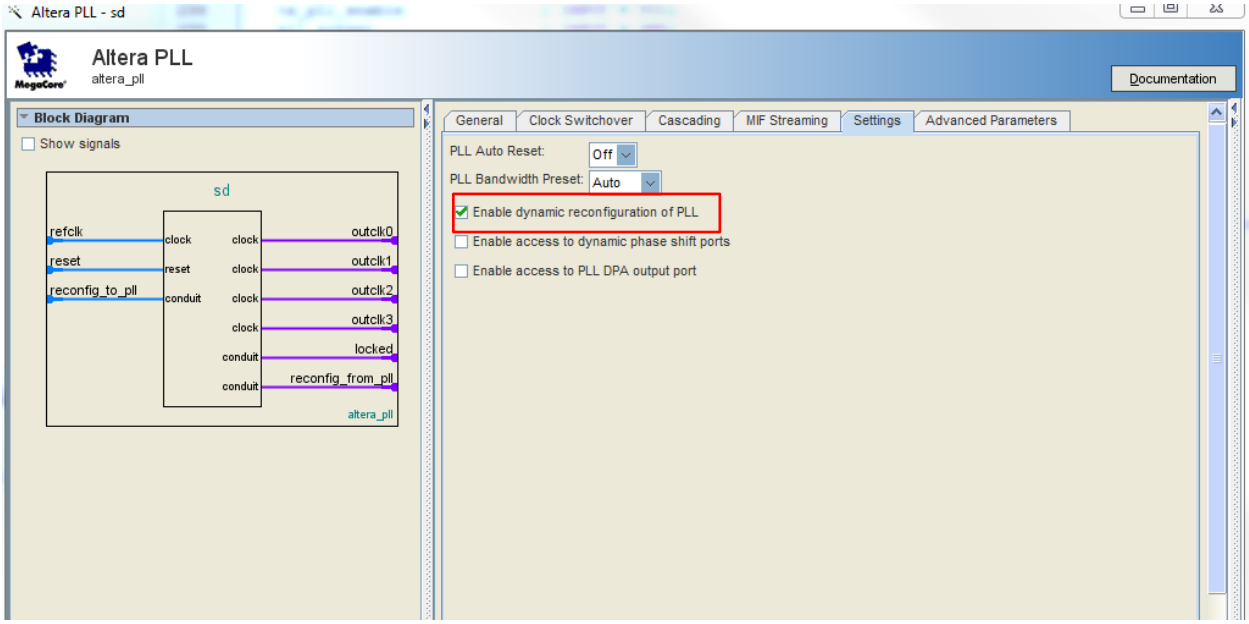

Figure 2-2. Altera_PLL megafunction with **Enable dynamic reconfiguration of PLL** turned on

3. Error Message

In the Quartus II software version 12.1 and onwards the connection shown in Figure 3-1 will produce a set of error messages for the ALTLVDS_RX connection (a design using an Arria V device is used for this example).

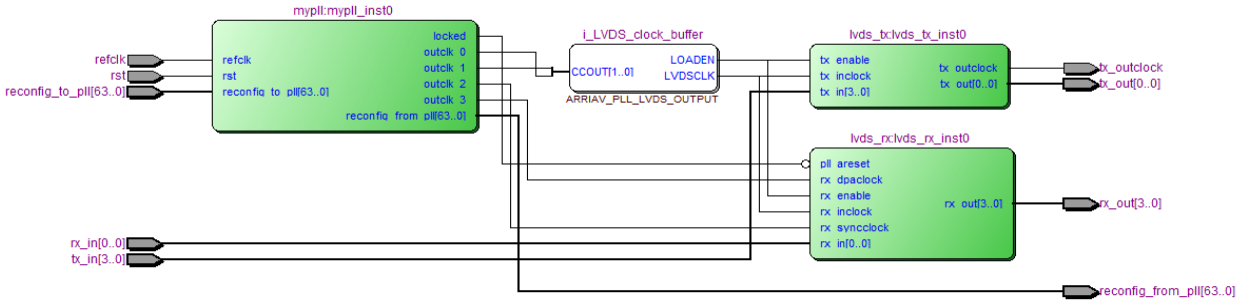

Figure 3-1. LVDS Interface with the Altera_PLL megafunction with DPA enabled in Arria V devices

ERROR messages produced by Analysis and Synthesis for ALTLVDS_RX

Error: SERDES DPA Block node 'lvds_rx:lvds_rx_inst0|altlvds_rx:ALTLVDS_RX_component|lvds_rx_lvds_rx:auto_generated|lvds_rx_dpa3' is not properly connected on the 'DPACLKIN' port. It must be connected to one of the valid ports listed below.

Info: Can be connected to PHOUT port of arriav_pll_dpa_output WYSIWYG

Info: Can be connected to OUTCLK port of generic_pll WYSIWYG

4. Workaround

a) Turn on the "**Enable access to the PLL DPA output**" option in the Altera PLL megafunction as shown in Figure 4-1 and the "phout" output port will be produced. The phout port is 8 bits wide.

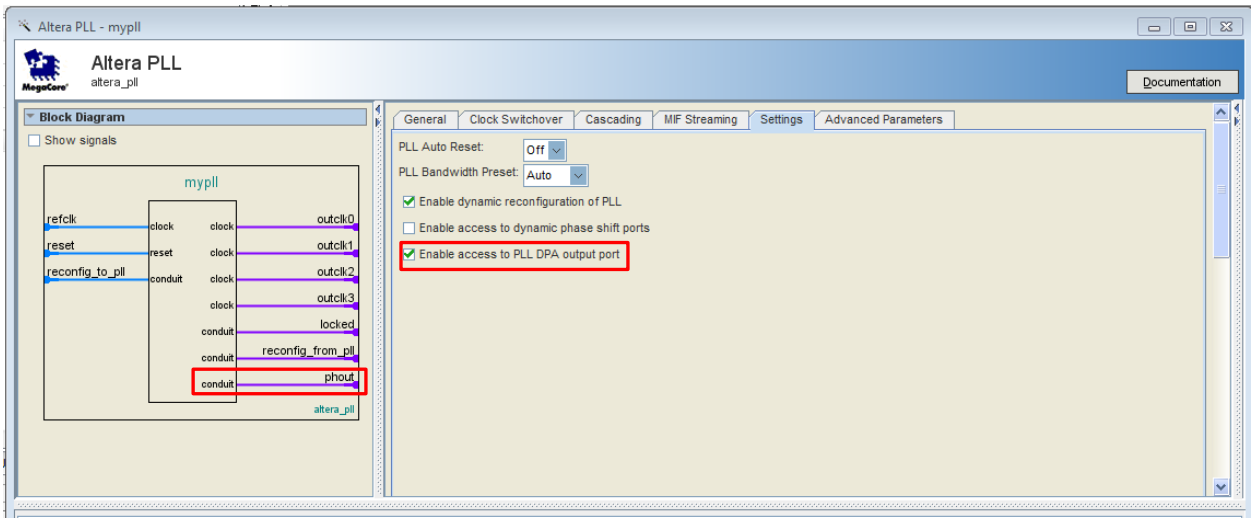

Figure 4-1 Altera PLL megafunction with **Enable access to PLL DPA output port** enabled

b) Turn on the "**Generate netlist**" option in the ALTLVDS_RX megafunction as shown in Figure 4-2.

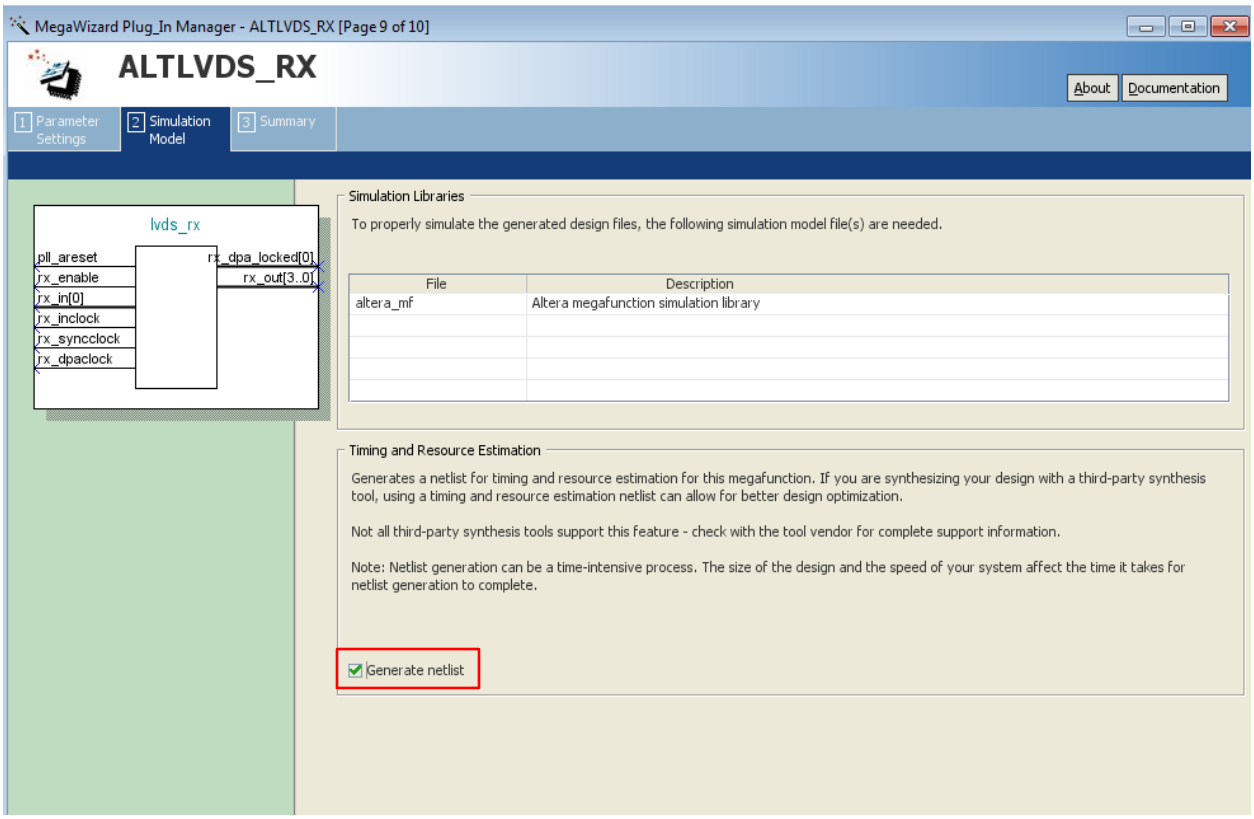

Figure 4-2: ALTLVDS_RX megafunction with **Generate netlist** enabled

c) In your project directory, delete the ALTLVDS_RX .v file, then rename the ALTLVDS_RX_syn .v file to ALTLVDS_RX .v.

d) Manually edit the ALTLVDS_RX .v to make all occurances of the “rx_dpaclock” port 8 bits wide as shown in Figure 4-3.

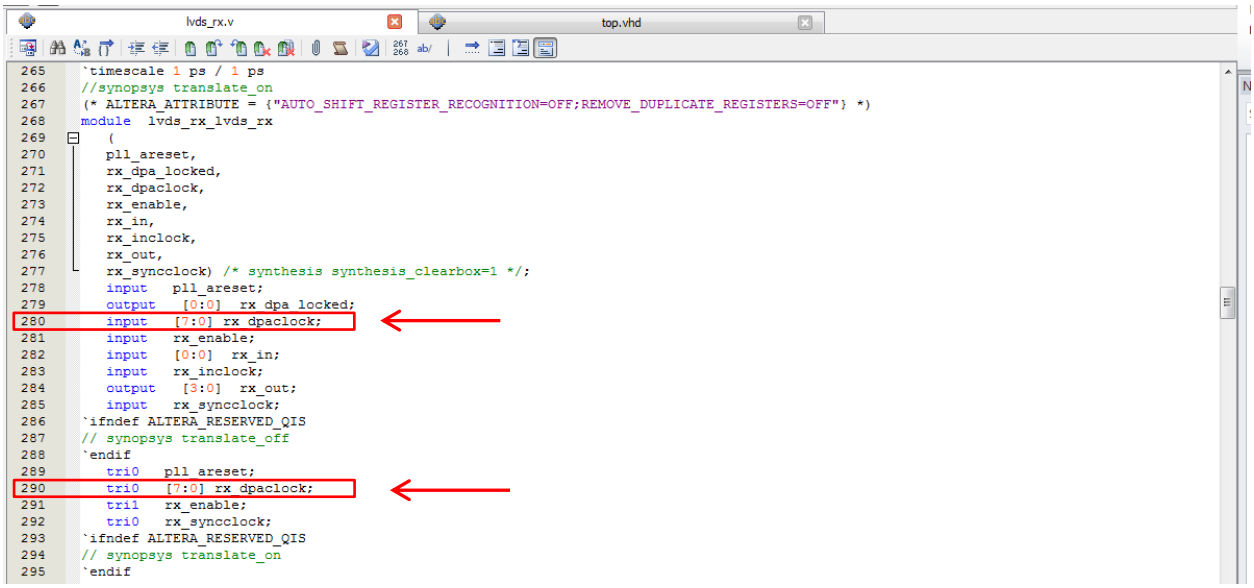

Figure 4-3: ALTLVDS_RX.v file modification

e) In your design, connect the PLL “phout” output to the ALTLVDS_RX “rx_dpaclock” input as shown in Figure 4-4.

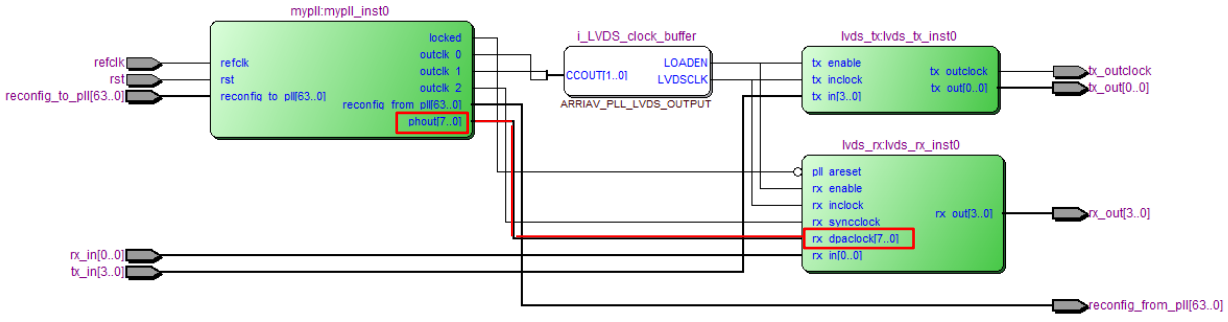

Figure 4-4: ALTLVDS_RX DPA mode design implementation

6. Conclusion

This document demonstrated how to implement and modify your design when using DPA mode in the ALTLVDS_RX megafunction when using external PLL mode. The design modification is required to avoid analysis and synthesis errors in the Quartus II software when using ALTLVDS_RX in external PLL mode with DPA enabled.

7. Revision History

Revision	Changes Made	Date
V1.0	Initial release.	September 2013