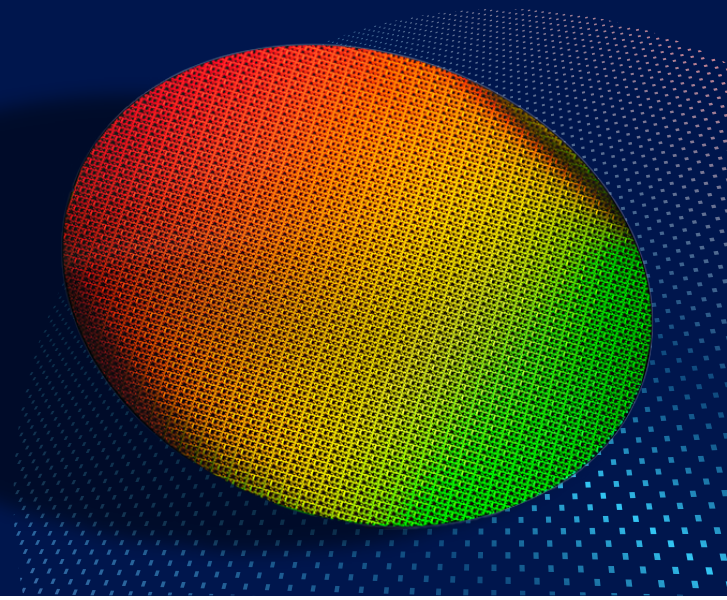
intel foundry

Technology Brief



Intel 18A Process Node Family

The Intel 18A process node family delivers an industry-first foundry platform built for modern compute workloads.

Contents

Intel 18A 1
Intel 18A-P 3
Intel 18A-PT 4
Spotlight 1: Power Boost 4
Spotlight 2: Power + Thermals 5
Ecosystem 6

What's New

- Updated Intel 18A-P performance and energy-efficiency metrics
- Measured performance from designs using PowerVia
- Insights into PowerVia's impact on routing, power integrity, and cost-effective scaling
- New figures illustrating PowerVia manufacturability, performance headroom, and thermal enhancements

From hyperscale data centers to power-constrained client and edge systems, today's designs demand higher performance per watt, predictable scalability, and architectures that are optimized for increasingly complex, multi-die systems.

Intel 18A represents a major advance in platform-level scaling, combining **RibbonFET** Gate-all-around (GAA) transistors with **PowerVia** backside power delivery in a production-ready foundry process. As the first foundry technology to bring both of these innovations into high-volume manufacturing, **Intel 18A** delivers significant gains in performance, energy efficiency, and area scaling over prior FinFET-based nodes.

Intel 18A-P builds on this foundation by adding a performance-optimized, design-compatible variant that unlocks additional power, performance, and area (PPA) for a broad range of modern workloads.

Intel 18A

RibbonFET Gate-All-Around Transistors

intel 18A

Intel 18A advances transistor architecture with the introduction of RibbonFET transistors (see Figure 1), the most significant transistor innovation since Intel introduced FinFET in 2011. RibbonFET improves electrostatic control, reduces leakage, and enables scalable drive current across operating points, delivering gains in performance efficiency and logic density.

These transistor-level improvements translate into platform-level benefits in routed designs with measurable increases in performance per watt, power efficiency, and chip density versus Intel 3 (see Figure 4).

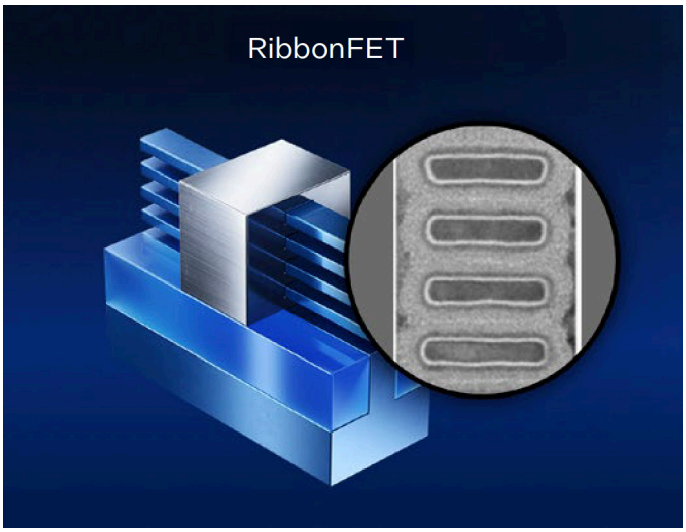


Figure 1. RibbonFET GAA transistor structure. Stacked ribbon channels fully surrounded by the gate enable dense, scalable transistor layouts with improved leakage control.

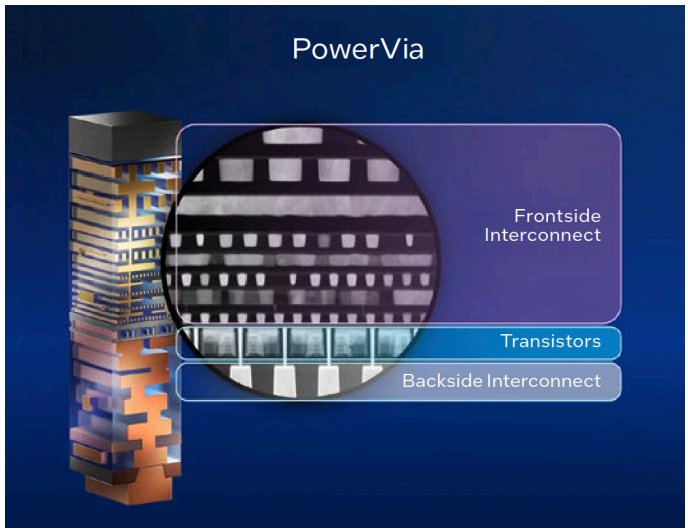


Figure 2. PowerVia backside power delivery. Backside interconnect layers deliver power directly to transistors, separating power and signal routing and freeing frontside metal resources.

PowerVia Backside Power Delivery

Backside power delivery is widely recognized as a performance innovation. Intel 18A extends its value by making it manufacturable, cost-effective, and design friendly.

PowerVia (see Figure 2) relocates coarse-pitch metals, power routing, and energy storage to the backside of the die, connecting directly to transistors using nano-scale through-silicon vias (nano-TSVs) embedded in each standard cell. This approach dramatically reduces resistive and inductive voltage droop while freeing critical frontside routing resources.

In routed logic designs, PowerVia delivers the following:

- **~10x reduction in worst-case dynamic voltage droop** compared to frontside power delivery (see Spotlight 2).
- **8–10%** routing closure improvement, enabling higher **cell utilization**.
- **6–11% block-level area compaction,** depending on power-grid assumptions.

Intel Foundry's backside power delivery avoids aggressive frontside metal pitch scaling. Direct-print extreme ultraviolet (EUV) patterning and relaxed signal pitch requirements **reduce mask count by up to 44% and process steps by up to 42% at two of the lowest signal-routing layers,** helping offset the cost of adding mature backside metal layers.[1]

RibbonFET + PowerVia: Improved CPU Performance

Compared to FinFET designs—where IR drop and interconnect delays mask expected transistor scaling benefits—CPU cores built with RibbonFET and PowerVia show a stronger frequency response as voltage increases. Production silicon results across multiple CPU designs confirm improved voltage to frequency scaling.

In addition, improved electrostatic control in RibbonFET transistors enables lower threshold voltage (Vt). This allows lower minimum operating voltage (Vmin) or higher frequency at the same voltage in lower supply voltage (Vcc) operation. Production silicon data shows that RibbonFET CPU cores with PowerVia deliver **~30% higher frequency at ~0.5 V** compared to FinFET designs (see Figure 3).[2] In low power applications, this architecture enables voltage reduction for the same performance, delivering significant voltage-driven power savings.

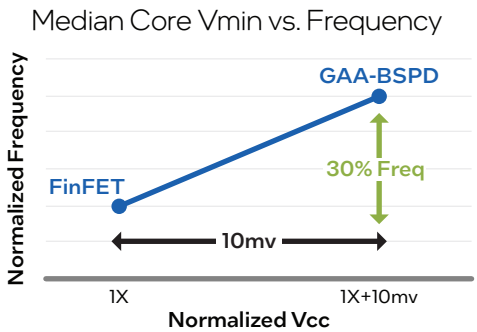


Figure 3. Approximately 30% frequency improvement at 0.5 V for CPU cores with RibbonFET and PowerVia vs. FinFET designs.[2]

Intel 18A Delivers		
18% performance per watt increase (at same power) vs. Intel 3	1.3x chip density improvement vs. Intel 3	38% power reduction (at same performance) vs. Intel 3

Figure 4. Intel 18A delivers improvements in performance and power efficiency compared to Intel 3.[3]

Omni MIM High-Density On-Die Decoupling

As advanced nodes support more dynamic, integrated workloads, stable local supply rails are critical. Tighter voltage margins and increased switching activity intensify power delivery demands in designs combining dense digital logic with analog, radio frequency (RF), and high-speed I/O.

Intel Foundry's Omni MIM technology (see Figure 5) integrates high-density metal-insulator-metal capacitors directly within the metal stack, delivering industry-leading announced **capacitance density (397 fF/μm²)** close to active circuitry. This localized charge storage reduces parasitic inductance, improves transient response, and stabilizes voltage during fast power events.

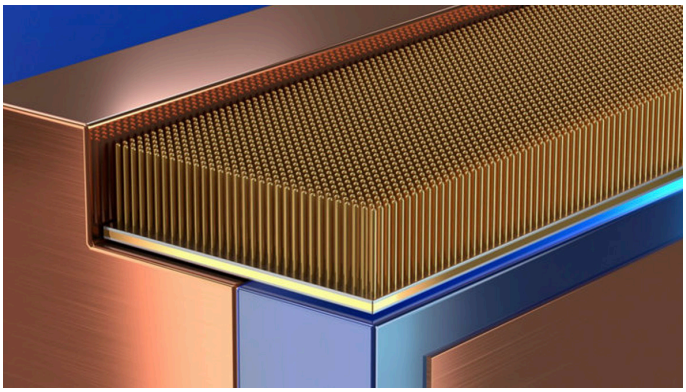


Figure 5. Omni MIM on-die decoupling capacitor structure.

Intel 18A-P

Intel 18A-P extends the benefits of RibbonFET and PowerVia with targeted improvements across transistor performance, interconnect efficiency, and platform optimization. Fully design-rule compatible with Intel 18A, Intel 18A-P enables customers to unlock additional PPA headroom without disrupting existing designs or flows (see Figure 6).

Gains are realized through a combination of newly added technology features and design technology co-optimization, rather than isolated device-level enhancements.

Intel 18A-P Delivers		
9% performance per watt increase (at same power) vs. Intel 18A	1x comparable chip density vs. Intel 18A	18% power reduction (at same performance) vs. Intel 18A

Figure 6. Intel 18A-P delivers improvements in performance and power efficiency compared to Intel 18A with full design-rule compatibility.[4]

RibbonFET and Device Enhancements

Intel 18A-P introduces new low-power and high-performance (HP) RibbonFET options across both HP and high-density (HD) libraries. Mobility-enhanced transistors at matched capacitance, combined with novel ultra-low-resistance contacts enabled by PowerVia (see Spotlight 1), deliver over **10% frequency improvement** for performance-optimized devices. Measured data shows **~5% NMOS and ~16% PMOS drive-current improvement,** alongside **20% and 12% reductions in external resistance,** respectively.[4]

Expanded logic Vt offerings and **33% tighter skew corners** provide designers with greater flexibility to tune speed, power, and leakage across a wide range of applications, from high-frequency compute cores to power-efficient system logic (see Table 1).[4]

Intel 18A Family Node Comparison				
	Intel 18A		Intel 18A-P	
Performance @ Iso-Power	1x		9% gain	
Library Height	180 nm	160 nm	180 nm	160 nm
Transistor	W2, W3	W1, W2, W3	W2, W3	W1, W2, W3
			W1 (Low Power)	W1.5 (Low Power)
			W3P (HP contact)	W3P (HP contact)
Vt	4 pairs of Logic Vts		5+ pairs of Logic Vts (New Logic Vt between ULVt and LVt)	
			10mV lower ULVt	
Skew Corners	Intel 18A Base Process		33% tighter skew corners	
Interconnect RC			V0-V2 R reduction; M2-M4 jogs	
Thermals			Improved thermal conductivity by 50%	

Table 1. Intel 18A-P technology feature enhancements compared to Intel 18A.[4]

Interconnect, Power Delivery, and Thermal Benefits

Interconnect enhancements in Intel 18A-P include improved via resistance in critical lower-metal layers and additional design-rule flexibility, contributing directly to improved routed performance and area scaling. These improvements build on the dramatically reduced dynamic voltage droop and improved routing efficiency achieved by removing the frontside power grid.

Thermal resistance of the overall stack is **improved by 20–40% on Intel 18A-P versus Intel 18A.**[1] The gains come from two key advances: ~50% higher bond stack thermal conductance through bonding layer engineering, and advanced thermally aware electronic design automation (EDA) flows that integrate thermal structures to better manage heat distribution at the design level.[4] Combined, the advances enable up to 40% lower delta temperature rise at high power density.[1] These enhancements are fully qualified for chip-package interaction (CPI) reliability using JEDEC standard stresses, supporting sustained performance in power-dense designs (see Spotlight 2).

Reliability and Design Readiness

Intel 18A-P builds on the proven reliability foundation of Intel 18A, meeting industry-standard level 1 wafer reliability targets. Intel 18A-P's mobility-driven performance enhancements also improve negative bias temperature instability (NBTI)-constrained performance/reliability tradeoff compared to Intel 18A, enabling faster transistors without compromising long-term reliability.

Mature EDA flows and design technology co-optimization (DTCO) methodologies ensure design ease of use while enabling customers to capture the full value of platform improvements.

Intel 18A-PT

Intel 18A-PT extends the Intel 18A platform to support advanced 3D integrated circuit (3DIC) architectures, including high-bandwidth memory (HBM) applications, combining backside power delivery with design-rule compatibility across the Intel 18A-P family. As an industry-first PowerVia-enabled base die, Intel 18A-PT adds pass-through and die-to-die through-silicon vias (TSVs) with hybrid bonding to support logic-stacking configurations. This enables tighter compute-memory integration, delivering lower interconnect latency and higher bandwidth density for data-intensive and performance-constrained systems (see Figure 7).

Intel 18A-PT Delivers		
~9x die-to-die bandwidth density vs. Intel 3-T	20-25% chip density increase vs. Intel 3-T	25-35% power reduction vs. Intel 3-T

Figure 7. Intel 18A-PT improves bandwidth density, chip density, and power efficiency compared to Intel 3-T (the base die derivative of Intel 3), offering a more capable base die for multi-chip packages.[5]

Spotlight 1: Performance Headroom on Intel 18A-P

Power Boost Technology for Frequency-Critical Compute

As workloads push frequency and responsiveness under tight power and thermal constraints, achieving higher performance without over-scaling voltage or area requires a broader set of tunable device options. Intel 18A-P expands the RibbonFET portfolio across both 180 HP (see Figure 8) and 160 HD libraries, giving designers finer control to balance the design's PPA.

At the top end of this expanded portfolio, **RibbonFET with Power Boost**—Intel 18A-P's performance-optimized dual contact device option (W3P below)—is engineered to increase available drive current through mobility enhancements and ultra-low-resistance contacts, translating directly into higher achievable frequency at matched capacitance. This device delivers over **10% frequency improvement on critical logic paths,** while complementary low-power and standard devices across both libraries allow the precise application of peak performance where it matters most without increasing power consumption.[4]

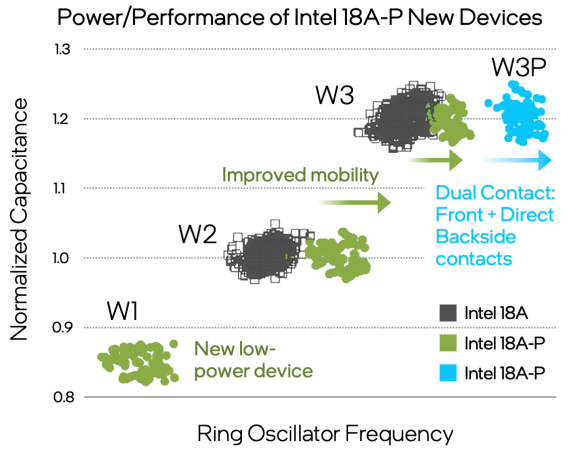


Figure 8. Updated 180 HP library devices. Power Boost (W3P) offers a high-performance option within a broader, tunable device portfolio.[4]

Segment-Specific Advantages

AI and High-Performance Computing (HPC)

AI and HPC workloads place sustained demands on performance delivery, power efficiency, and timing margin under load. Intel 18A-P extends the Intel 18A platform with additional optimization headroom through expanded logic Vt options, including an intermediate Vt and tighter skew control, enabling more precise tuning across HP and energy-efficient operating points. These capabilities improve achievable frequency and efficiency in fully routed designs.

New low-power and HP device options further enhance scalability for HPC and AI systems. Reduced-capacitance devices improve efficiency in dense logic, while HP transistors with mobility enhancements and low-resistance contacts deliver over **10% frequency improvement** at matched capacitance.[4] Combined with advanced SRAM offerings that are optimized for low-Vmin operation, Intel 18A-P enables CPUs, GPUs, and AI accelerators to integrate compute and on-chip memory more efficiently, supporting higher throughput and sustained performance for data-intensive workloads.

Mobile, Client, and Edge

Mobile and baseband processors must operate efficiently across wide and dynamic voltage ranges while maintaining predictable performance and thermal behavior in highly integrated designs. Intel 18A-P provides expanded device and library flexibility, enabling designers to optimize PPA across multiple operating modes without over-constraining the system.

Low-capacitance device options, including minimum- and intermediate-width transistors in both HP and HD libraries, improve energy efficiency for dense logic operating at lower voltages. Combined with expanded logic Vt options and improved Vmin characteristics in both logic and SRAM, Intel 18A-P supports efficient compute and signal-processing blocks that adapt smoothly to changing workload demands. These capabilities reduce power consumption and thermal load.

Spotlight 2: Power Integrity and Thermal Management

Backside Power Delivery for Sustained Performance

Across HPC and AI, mobile and edge devices, aerospace and defense systems, and vision-centric designs, reduced voltage droop is critical to predictable performance. Intel 18A delivers significantly lower dynamic voltage droop, while Intel 18A-P further reduces temperature rise at high power density—supporting sustained operation in thermally and power-constrained environments.

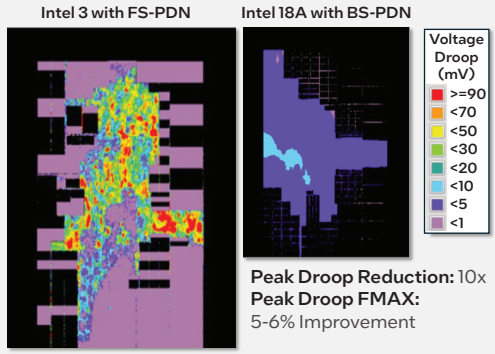


Figure 9. Power supply droop heatmaps for CPU core implementations. Intel 18A with backside power delivery demonstrates 10x reduction in dynamic voltage droop vs. Intel 3 with frontside power delivery.[1]

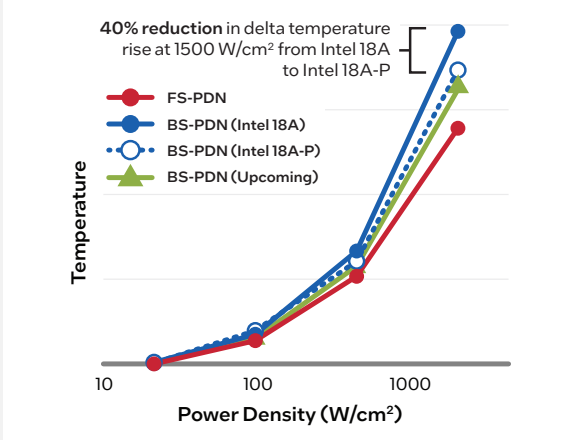


Figure 10. Temperature vs. power density for backside power delivery nodes. Intel 18A-P shows up to 40% reduction in delta temperature rise compared to Intel 18A, highlighting improved thermal management for HD designs.[1]

Aerospace, Defense, and Government Services (ADG)

The ADG sector increasingly relies on advanced computing to support autonomous systems, battlefield analytics, space-based AI, and cybersecurity—often under stringent size, weight, power, and cost (SWaP-C) constraints. Intel 18A and Intel 18A-P address these needs with improved power efficiency and predictable performance in power-constrained environments, supporting mission-critical designs that demand both capability and robustness.

Integrated Omni MIM capacitors improve on-die decoupling and power integrity, reducing voltage fluctuations and power-supply-induced jitter. Fully isolated body transistors and flexible multi-Vt device options further enable low-leakage, low-voltage circuit designs that are optimized for energy-efficient operation.

Intel 18A-P improvements in reliability and long-term performance stability support sustained operation across extended mission profiles. Enhanced power delivery, improved device lifetime characteristics, and mature design enablement reduce sensitivity to voltage, thermal, and aging effects over time.

Image Signal Processing, Video, and AI Vision

Image signal processing, video, and vision-centric AI workloads place strong emphasis on power efficiency, real-time responsiveness, and high integration density in compact form factors. Intel 18A and Intel 18A-P support these requirements by enabling improved power integrity and routing efficiency in densely integrated designs, reducing power loss and supporting more consistent real-time performance in routed implementations.

Area-efficient logic and memory integration enabled by RibbonFET allows designers to incorporate additional functionality within constrained die footprints, supporting compact systems such as portable medical devices, industrial sensors, and embedded vision platforms. Improved efficiency at lower operating voltages further supports reliable, scalable processing in battery-operated and power-limited environments.

Tap into the Intel Foundry Ecosystem

The **Intel Foundry Accelerator Alliance** helps customers turn their innovations into silicon by leveraging the world-class capabilities of partners from across the design ecosystem, including intellectual property (IP), proven tools and flows, cloud capabilities, and design acceleration services.

Supported by mature EDA flows, Intel 18A and Intel 18A-P are compatible with advanced packaging technologies such as Embedded Multi-die Interconnect Bridge (EMIB) and Foveros, enabling scalable multi-die systems optimized at both the die and system level.



Services Across the Lifecycle

Prototyping services enable rapid design validation on advanced process nodes, helping teams move from concept to silicon efficiently. Through **multi-project wafer (MPW) shuttles,** customers gain cost-effective access to leading-edge technologies for early-stage designs, reducing time-to-market while optimizing resources. In addition, specialized enablement teams provide hands-on support across the entire lifecycle, ensuring quality, compliance, and performance requirements are met for highly demanding environments.

Transform Your Silicon Vision into Reality

Intel Foundry offers full-stack solutions that reduce design risk and increase confidence from concept to production. Our integrated approach combines cutting-edge process node technologies—from mature nodes to leading-edge processes—with revolutionary advanced packaging solutions and select systems technologies.

Ready to revolutionize your next-generation products? Visit intel.com/foundry.

intel foundry

[1] E. Karl et al., "Backside Power: Enabling Energy-Efficient Performance on Advanced Node Designs," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[2] M. Shamanna et al., "CPU Cores in GAA with Backside Power: Silicon-Validated Design Insights," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[3] K. Fischer et al., "Intel 18A Platform Technology Featuring RibbonFET (GAA) and PowerVia for Advanced High-Performance Computing," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2025.

[4] A. Bowonder et al., "Intel 18A-P CMOS Technology Enhancement Featuring Advanced RibbonFET (GAA) Transistors and PowerVia for High-Performance Computing," IEEE/JSAP Symposium on VLSI Technology and Circuits, June 2026.

[5] Based on Intel internal analysis comparing Intel 18A-PT to Intel 3-T as of April 2025. Results may vary.

Performance varies by use, configuration, and other factors. Results may vary.

All product and service plans, roadmaps, and performance estimates are subject to change without notice. Projections about future node performance and other metrics are inherently uncertain. Performance results are based on testing as of dates shown. Your costs and results may vary.

This document contains forward-looking statements about Intel's future plans or expectations, including its process technology roadmaps. These statements are based on current expectations and involve many risks and uncertainties that could cause actual results to differ materially from those expressed or implied in such statements. For more information on the factors that could cause actual results to differ materially, see our most recent earnings release and SEC filings at www.intc.com.

Intel® technologies' features and benefits depend on system configuration and may require enabled hardware, software, or service activation. Performance varies depending on system configuration. No product or component can be absolutely secure. Check with your system manufacturer or retailer or learn more at www.intel.com.

All information provided here is subject to change without notice.

© Intel Corporation. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Other names and brands may be claimed as the property of others. 0626/DBAD/KC/PDF 367370-001US