

Clear CMOS after Hardware Configuration Changes

Technical White Paper

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2 337986-001



Contents

1	Introdu	ction	5	
2	Clear C	MOS – When and Why	6	
	2.1	BIOS Update Completion	6	
		Replaced Processor		
	2.3	Any Replaced DRAM Module	6	

337986-001



Revision History

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337986	001	Initial Release.	August 2018

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4 337986-001



1 Introduction

CMOS is a small amount of memory on a computer motherboard that stores the BIOS settings. To bring up a system in a most efficient way with the minimum boot time, the system BIOS saves settings in the CMOS RAM based on the hardware configurations of previous boot.

Intel recommends clearing CMOS for the following scenario:

- For BIOS update completion. Refer Section 2.1
- For Replaced Processor. Refer Section 2.2
- For any Replacement of DRAM Module. Refer Section 2.3

The above recommendations apply to Intel's 6th, 7th and 8th Generations.

Note: It is assumed that the above procedure as part of normal practice during a system upgrade or in a manufacturing line.

Refer to Intel support article $\frac{\#000025368}{}$ and/or the motherboard user manual on how to clear CMOS.

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337986-001 5



2 Clear CMOS – When and Why

A clear CMOS procedure is performed, it restores the BIOS default settings and prevents BIOS accidently applying invalid settings to new hardware obtained from the ones previously installed on the system.

2.1 BIOS Update Completion

After completion of a BIOS update, there may be a CMOS checksum error or other problems due to CMOS data being corrupted. Performing a Clear CMOS will correct those errors.

2.2 Replaced Processor

The system BIOS detect the processor capabilities and configures it for best performance or max power saving per user preference. In most of the cases, the BIOS is able to detect a new processor being installed via CPUID signature. However, if the new processor has identical CPUID signature as the one being replaced, the BIOS is unable to tell the processor has been swapped.

In this case, if the newly installed processor has different capabilities than the old one, such as Max Turbo Frequency, the BIOS will apply the settings obtained from the old processor to the new processor, result in performance impacts or even a boot issue.

2.3 Any Replaced DRAM Module

The MRC trainings initialize the memory controller and finding the optimize memory read/write timings for best performance with lowest power. The MRC trainings data from the first cold boot is save in the CMOS and restored for next boot assuming no DRAM configurations change. When a DRAM module is physically removed and/or replaced, there might not be enough indications, same DRAM silicon chips with different module manufacture for example, to trigger a fresh MRC training. In this case, the hardware deviations were not taking into account and result in performance impacts or even a boot issue.

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6 337986-001